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REDUCTION IN SUSCEPTIBILITY OF MOS DEVICES TO RADIATION- AND ELECTRICALLY-INDUCED DEFECTS

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14. ABSTRACT

The goal of this project was to identify fabrication techniques by which the susceptibility of Metal-Oxide-Semiconductor devices to the Negative-Bias-Temperature Instability (NBTI) and to radiation damage could be reduced. To that end, two techniques were attempted. In the first attempt, helium ions were implanted into the oxide layer of the devices in an attempt to frustrate the formation of defects via hydrogen depassivation. This attempt was not successful, perhaps because defects are not generated via hydrogen depassivation, or because the hydrogen does not come from the oxide bulk and hence cannot be easily blocked. The second attempt was to repair missing oxygen centers at the interface between the silicon substrate and the silicon dioxide insulating layer by annealing the devices in oxygen using rapid thermal processing techniques. This attempt was also not successful. However, there was insufficient time to optimize the parameters of the anneal, and we remain hopeful that future work may reveal that this method is, in fact, viable. Although we were unable to develop fabrication techniques to mitigate damage, we nevertheless were able to draw some important conclusions concerning the nature of defects induced by Negative Bias-Temperature Stress. In particular, we developed a model in which a positively charged defect exists in a shallow trapping site in the oxide very near the silicon substrate, and that the population of this positive charge is in dynamic equilibrium with the substrate, requiring both elevated temperature and inversion bias to exist. In addition, measurements of these defects on Metal-Oxide-Semiconductor Field Effect Transistors fabricated with HfSiON insulators were made. These measurements showed that positive charge may be channeled into shallow defects between the oxide and HfSiON layers, and removed from the device insulator by the voltage applied to the drain of the device. This conclusion was based on the observation that devices operated in the saturation region, where the drain bias is large, show less damage than devices operated in the linear region, where the drain bias is small. The result has implications for the measurement of NBTI defects.

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1.0 SUMMARY

The goal of the project is to identify fabrication treatments that may reduce the susceptibility of Metal-Oxide-Semiconductor (MOS) devices to defect generation under operating conditions involving electrical stress or radiation. The treatments tested were (i) implantation of He ions into the oxide and (ii) post-oxidation anneal in oxygen. The ion implantation method was unfortunately not effective. The oxygen anneal was inconclusive; however, we remain optimistic that this technique may prove useful, and we suggest that such experiments be continued.

While we were not successful at finding fabrication procedures that are effective in reducing defect generation, we were successful in observing several interesting properties of Negative-Bias-Temperature Stress (NBTS)-induced positive charge in MOS oxides. These observations led to a model of the charging process that to our knowledge has not been elucidated in the literature.

In addition to establishing a model for NBTS-induced charging, we observed that charging in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is dependent on the mode in which the MOSFET is operated: when operated in saturation mode, a MOSFET will experience less damage than when operating in the linear regime. This observation resulted in a publication in the journal *Microelectronic Reliability*.

2.0 INTRODUCTION

The scaling of high-performance MOS devices to the nanometer level has been accompanied by immense challenges in fabrication, as well as an unprecedented attention to device physics and reliability concerns. Modern integration levels, and concomitantly reduced device sizes, have resulted in increased oxide electric fields, and in increased chip temperature.

Principal among reliability concerns brought about by increasing oxide electric fields combined with elevated device temperature is the Negative-Bias-Temperature Instability (NBTI). In accelerated testing measurements in which moderate negative bias (a few MV/cm) and temperatures in the range 100 ^{o}C – 200 ^{o}C are applied, MOS devices are observed to sustain damage in the form of positive charge formation and interface state generation. The extent of the damage increases with increasing bias and temperature, although the details are different depending on the sample fabrication history. For an excellent overview we refer to the article by Stathis.[1]

The author has been interested in the phenomenon of positive charging in MOS devices for some time. He has in particular been a proponent of the idea that positive charge can manifest itself in at least two types of defects, with very different electrical properties. [2] These defects are referred to as the trapped hole and the anomalous positive charge (APC). Until the present work, however, he had not explored the NBTI-induced defect, which is also positively charged.

This work attempts to learn the nature of the NBTI defect and its relationship to the trapped hole and APC, and from that knowledge to develop MOS fabrication methods to reduce the susceptibility of these devices to damage induced by NBTS and radiation. The interest in radiation stems from the fact that exposure to ionizing radiation also results in positive charging

and interface state generation. In the case of radiation, the positive charge species is predominantly trapped holes, but it was anticipated that there may be a connection between radiation exposure and NBTI.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

Here we describe our experimental procedures and methods along with any assumptions made. In particular we do this for the sample fabrication, capacitance-voltage measurements, NBTI measurements, and tests for anomalous positive charge and trapped holes.

3.1 Sample Fabrication

MOS capacitors were fabricated at the University of Houston, and comprise the majority of samples described in this report. However, in Section 4.4 below we describe the results of measurements made on MOSFETs provided by Dr. Roderick Devine.

MOS capacitors were fabricated according to accepted standards, and using recipes in use at our facility. Table 1 indicates the details of the fabrication process; oxides were thermally grown in a conventional oxidation furnace on n-type (100) silicon substrates (doping density ~1 x 10^{15} cm^{-3}) according to the prescription in Table 1.

Following oxidation, samples were placed in a vacuum chamber, and 99.999% pure aluminum was used to deposit gate electrodes by evaporation through a shadow mask. The gate electrodes area is 2.6 x 10^{-3} cm^2.

For the oxygen anneal experiments described in Section 4.5, we metallized capacitors from Si wafers purchased from University Wafer. These wafers had 30 nm of thermal SiO_2 grown by University Wafer. Aluminum gates were deposited at UH after post-deposition processing in a Rapid Thermal Processing (RTP) unit, as described in Section 4.5. Use of an external supplier was necessary because during that time, our furnace facilities were not producing oxides reliably. There was no cost to the project for these wafers.

Table 1. Thermal oxidation conditions (typical furnace conditions).

Treatment	Temp (^oC)	Time (s)	Ambient	Comment
Pretreatment	1000	3600	3% TCE/N2	Furnace clean
Insertion	1000	120	N2	
Oxidation	1000	1500	O2	
Post-Ox Anneal	1000	3600	N2	reduce “fixed” charge
Removal	1000	120	N2	—
Metallization	23	-	Vacuum	Al thermal deposition
Post-Metal Anneal	450	600	N2	reduce interface states

3.2 Electrical Measurements: Capacitance-Voltage

Capacitance-voltage (CV) measurements made on MOS capacitors were used for basic characterization, and in particular to define the state of the oxide in terms of charge trapping and interface state generation. These measurements were made according to accepted practice as described in reference [3]. Measurement facilities at UH for this purpose include an HP 4284A LCR meter for high frequency CV measurements. The 4284A is capable of measuring capacitance over the frequency range 20 Hz to 1 MHz. In general, high frequency CV measurements described in this work were made at 100 kHz in either the parallel or series resistance mode. In the work discussed here, there was no difference in the results obtained using these two modes.

High frequency CV measurements can be used to find (i) the oxide thickness, (ii) the substrate doping density, (iii) the flatband capacitance, and (iv) the flatband voltage. From the flatband voltage one can determine the charge present in the oxide. We refer the reader to reference [3] for details.

Quasi-static CV measurements were used to extract interface state density. For this purpose we used an HP 4140B IV voltage source/current meter. This test station applies an analog voltage ramp to the sample, and simultaneously measures current. The result is a measurement of the dc capacitance, which is equivalent to the low frequency capacitance [reference 1 pp. 603 – 604]. A comparison of the high- and low-frequency (or quasi-static) CV curves reveals the density of interface traps in the Si band gap. Again, we refer the reader to reference [3] for details.

The measurement equipment in our lab is controlled using LabView software written in-house. The same software is used to analyze data; for example, to extract interface states from the capacitance data.

For all capacitor measurements discussed here, samples were placed in a light-tight sample chamber manufactured by Signatone, and on a sample stage capable of elevated temperature to 500^{o}C. The samples were probed using MicroManipulator probe stations. The hot stage was water-cooled for rapid return to room temperature.

High-and low-frequency (quasi-static) CV measurements, as well as the interface trap density extracted from their comparison, are shown in Figure 1 for a sample before and after a post-metallization anneal (PMA). Figure 1a shows the high frequency data; Figure 1b shows the quasi-static data; Figure 1c shows the resulting interface trap density. The sample was not exposed to stress. Note the dramatic reduction in interface states following the PMA. This phenomenon is well known in the literature, and is due to passivation of interface states by hydrogen generated during the PMA process.

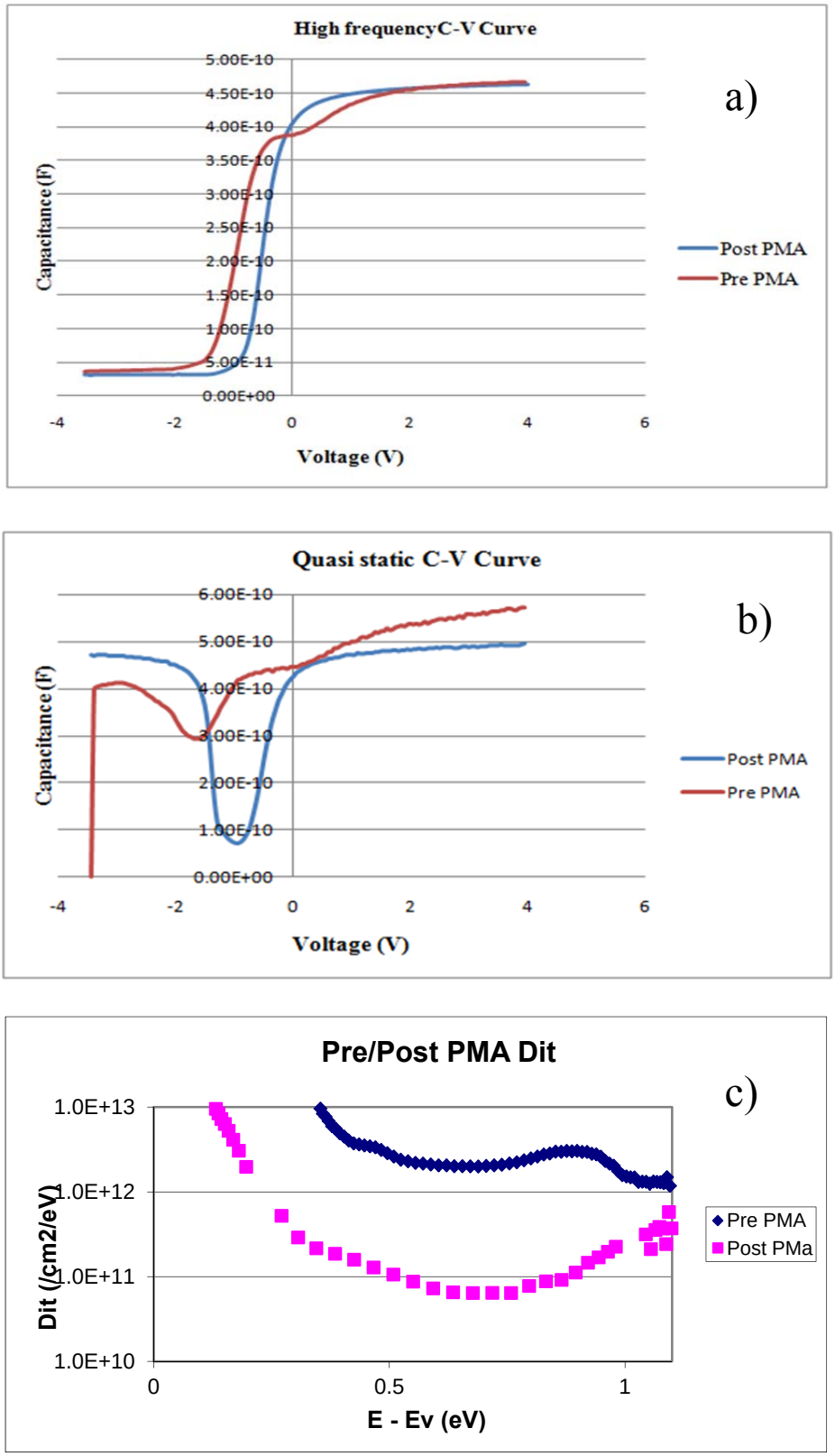


Figure 1. a) High-frequency CV data; b) Quasi-static CV data; c) Interface trap density extracted from the CV data, before and after post-metallization-anneal.

3.3 Electrical Measurements: Constant Voltage Stress and NBTI

The stress technique employed in this work is NBTS: Negative-Bias-Temperature Stress, which reveals the presence of the Negative-Bias-Temperature Instability. This test is performed with the device connected to the CV apparatus, as if a CV measurement were to be made. However, instead of making a CV measurement, a constant negative bias corresponding to strong inversion is applied for a fixed time. The sample chuck is elevated in temperature, and flatband voltage measurements are made at pre-determined time intervals. The flatband voltage measurement is in essence a CV measurement made by determining the voltage required to achieve the flatband capacitance.

The protocol for the NBTI stress measurement is as follows.

i. A CV curve is measured at room temperature to determine the initial state of the sample, including oxide charge and interface state density.
ii. A negative bias (the stress bias) corresponding to the desired stress field (typically -4 to -6 MV/cm) is applied at room temperature.
iii. Following a pre-determined time interval Δt (typically 60 – 150 s), a flatband voltage measurement is made. The stress bias is then re-applied.
iv. After several time intervals at room temperature, when room-temperature instabilities have settled out and initial conditions have been established, the temperature is raised to the desired stress temperature (typically 100 – 175^{o}C).
v. Flatband voltage measurements are made at the pre-set time interval for as long as the stress test is to be carried out. The sample is then returned to room temperature.
vi. A CV measurement is made at room temperature following stress to determine the final state of the sample. In addition, other tests may be done on the stressed sample to examine the resulting defects.

The flatband voltage measurement is made as follows.

i. After a pre-determined time interval Δt, during which the stress voltage is applied, the voltage across the capacitor is changed to the most recently measured flatband voltage.
ii. The capacitance is read from the capacitance meter. If the capacitance is higher than the flatband capacitance, it means that the CV curve has shifted to more negative voltage. If it is lower, it has shifted to higher voltage. (This is the case for n-type substrates, which are the only substrate types reported here. For p-type substrates, the opposite would be true.)
iii. The applied voltage is adjusted in intervals of 10 mV in the direction necessary to approach the flatband capacitance; the capacitance is measured at each step until the flatband capacitance is reached. Interpolation is used if the last voltage step overshoots the flatband capacitance.
iv. Once the flatband capacitance has been recorded, the stress voltage is reapplied.

Measurement of the flatband voltage by this method takes approximately 1 second in most cases.

3.4 Electrical Measurements: The Test for Anomalous Positive Charge and Trapped Holes

As described below in Section 4.1.2, we tested some of the capacitors for the presence of APC following NBTS. The signature of this defect is that it exchanges charge with the Si substrate, just as interface states do, but it does so over a much longer time period: from minutes to hours. As for interface states, the charge exchange is reversible in that charge may be moved in or out of the defect, depending on the sign of the bias applied to the gate electrode.

To test for the presence of APC, a moderate voltage is applied to the sample (2 – 4 MV/cm), and the flatband voltage is monitored as a function of time, as described above. Indeed, this is the same protocol as for the measurement of NBTI defects, except that the stress field is typically lower than for NBTI, and the measurement is made at room temperature instead of elevated temperature. If APC is present, it manifests itself as a slowly changing flatband voltage. The sign of the probe voltage is alternated between positive and negative so that if APC is present, it will manifest itself as a reversible exchange of charge. Examples of this behavior can be seen in Section 4.1.2.

The protocol just described can also be used to test for the presence of trapped holes. The signature of trapped holes is quite different from that of APC. Trapped holes will be depleted from the oxide if a positive gate bias is applied, but will not return under negative bias. Thus, instead of observing a charge/discharge cycle as for APC, only a discharge process is observed. Further, the discharge of trapped holes is considerably more rapid (seconds to minutes) than that of APC (minutes to hours).

An example of the application of this test, for APC and trapped holes, is shown in Figure 2. Figure 2 shows results of this test performed on a control sample (upper curve) and on samples that were previously subjected to two different stressing protocols: positive and negative high field bias (~7 MV/cm). Note that the stress experiments are not shown; what appears in Figure 2 is only the result of the test to look for APC or trapped holes, carried out *after* stress is complete. The label "FNT" refers to the high field stressing, which is typically known as "Fowler-Nordheim Tunneling". The stress resulting in the center curve was the positive bias FNT, which is known to produce APC. The stress resulting in the lower curve was negative FNT, which is known to produce trapped holes.

The test for APC and trapped holes was performed at an alternating bias of +/- 4.5 MV/cm in Figure 2. The APC charge/discharge cycle is clearly observed in the middle figure, where the flatband shift moves back and forth symmetrically: flatband voltage (V_{fb}) moves downward when negative bias is applied, which discharges APC defects by forcing electrons out of the defect and into the substrate; it moves upward when positive bias is applied, which causes APC defects to again be populated by electrons. The lower curve is typical of trapped holes, in which the overall movement of the curve is upward, i.e., non-symmetric. This happens because under positive bias, holes are removed from the sample, but the process is not reversible (although there appears to be a small component of APC in this sample as well, so there is some downward movement for negative bias.)

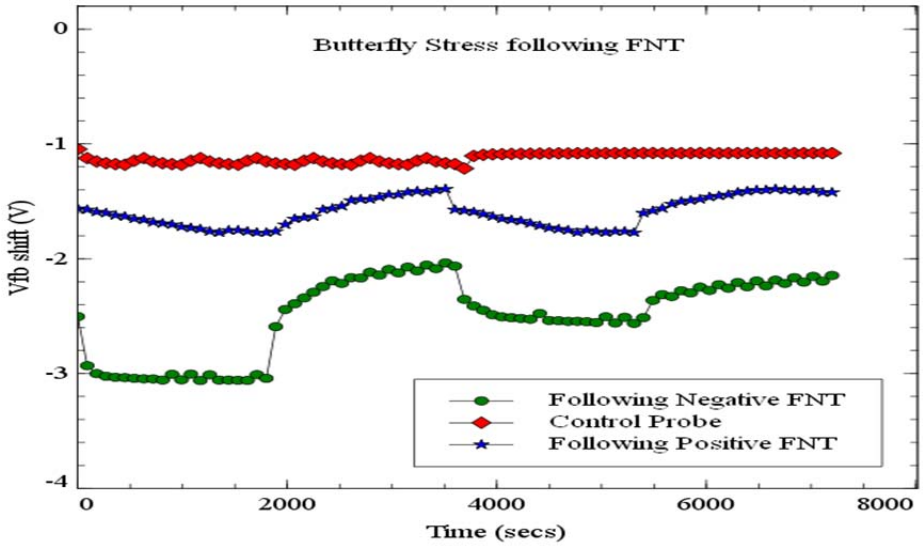


Figure 2. Illustration of the behavior of trapped holes and APC.

A photograph of the measurement apparatus is shown in Figure 3. Sitting on top of the rack to the left is a Keithley 220 Current Source used for constant current injection experiments, which are not reported here. Next to the current source is a programmable multimeter. The HP 4284A is located inside the rack, in the upper position. Below it in the rack is the HP 4140B. The sample stage and hot chuck are inside the black box. A microscope used to position the probes is shown above the sample stage. The electronics for heating the sample stage are not shown.

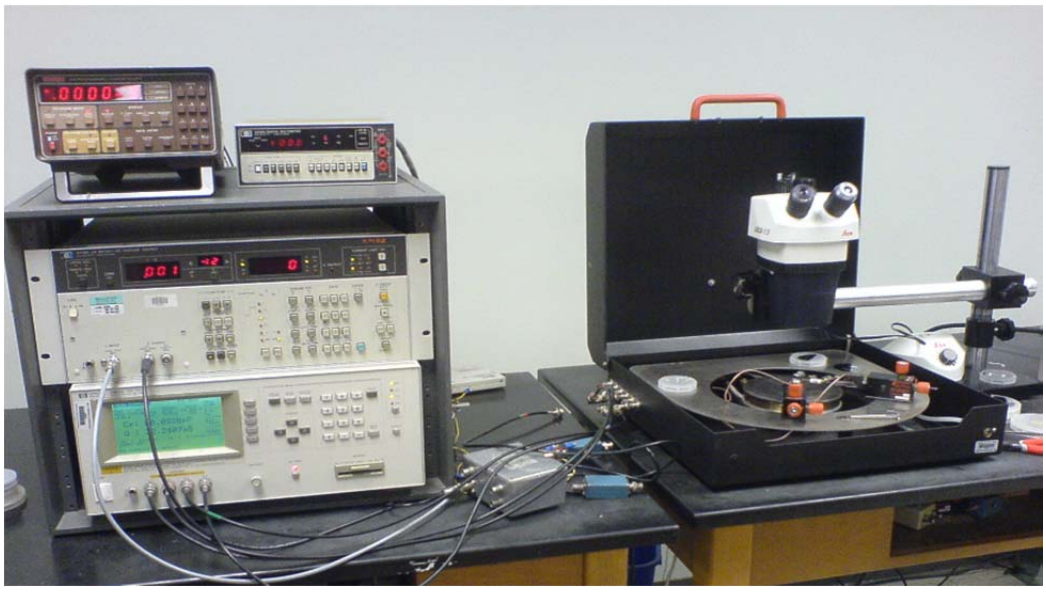


Figure 3. MOS measurement station at the University of Houston.

4.0 RESULTS AND DISCUSSION

In this section we list and explain in detail the principal accomplishments for the project. For each section, we present a brief summary, followed by presentation of the data and analysis justifying each accomplishment.

4.1 Nature of Positive Charge Generated by NBTI

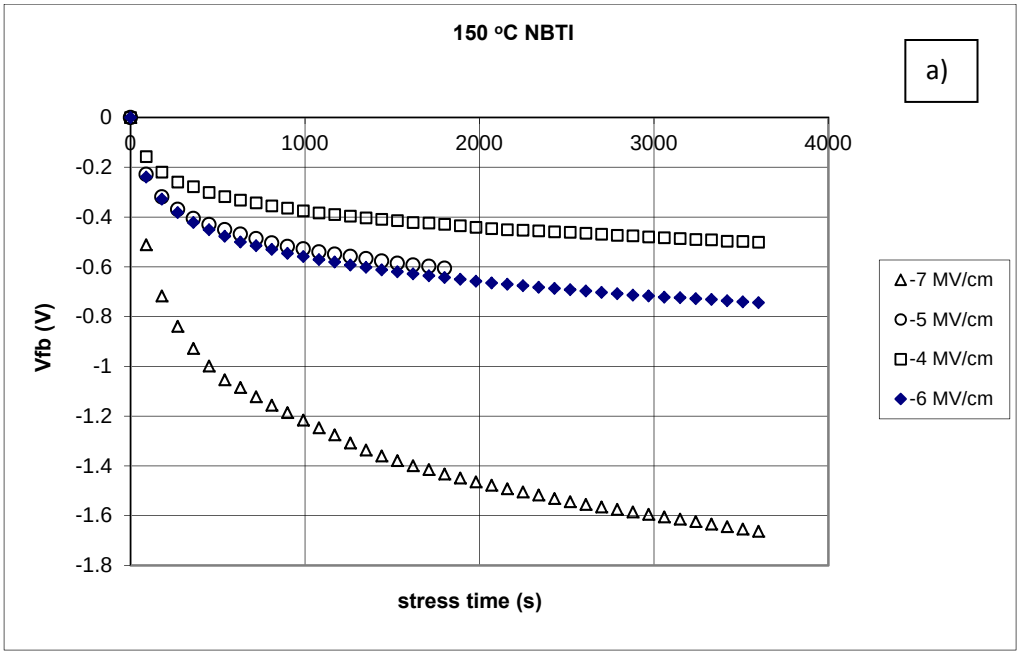
NBTI stress creates both interface states and trapped charges in the MOS capacitor or MOS field effect transistor gate dielectric. Here we describe the nature of this charge beginning with a basic characterization. We then analyze the charge/discharge kinetics and temperature/bias dependence of the charge population.

4.1.1 Basic Characterization of NBTI-Induced Charging and Interface States

In this section we show the kinetics of NBTI charging as determined by tracking of the flatband voltage as a function of time under NBTI stress. We also show the results of interface trap measurements made using a high/low frequency capacitance-voltage comparison.

We conducted a series of NBTI measurements under conditions similar to those reported in the literature. In these experiments, a negative dc voltage corresponding to -4 to -7 MV/cm is applied to the gate of a MOS device for an hour or more while the device is held at temperatures ranging from 100 to 200^{o}C. This procedure creates positive charge, which is detected as a change in flat band voltage V_{fb}. It also creates interface states, which we measure using a comparison between the quasi-static and high frequency CV curves.

We show in Figure 4a NBTI data taken at 150 ^{o}C and for oxide fields of -4, -5, -6, and -7 MV/cm. The data show the *change* in the flatband voltage (i.e., the first data point has been set to 0) vs. time. As a control, we measured the flatband voltage shift of samples exposed to the same oxide fields, but at room temperature. These data are shown in Figure 4b. We find a negligible shift, except for the -7 MV/cm case. Evidently there is some damage at room temperature for this field, although it is still significantly less than at 150^{o}C. So as not to generate damage by field alone, we did not use fields larger in magnitude than 6 MV/cm following this test.



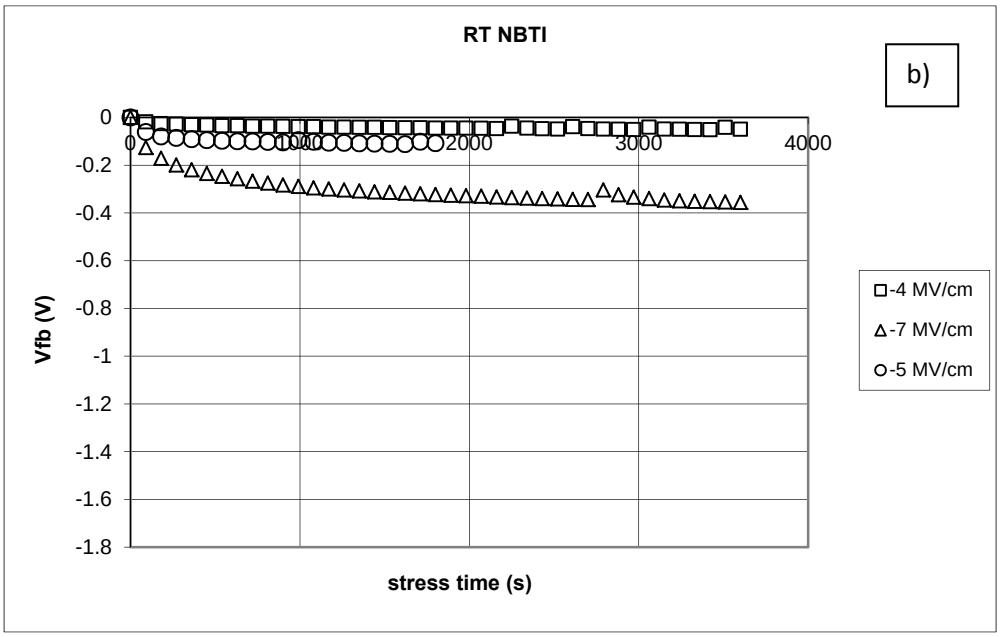


Figure 4. a) NBTI data taken at 150 °C and the oxide fields indicated in the legend. b) Data taken at 300 K and the same oxide fields as in the NBTI data of Figure 4a.

As a means of characterizing NBTI defect generation kinetics, many researchers have fit NBTI data such as that in Figure 4a using power-law kinetics. We have done that as well, with the results shown in Figure 5a for the -6 MV/cm data, and in Table 2 for all four curves. The exponents in the table are typical of literature values. We note that an equivalent areal defect density can be extracted from the flatband shift ΔV_{fb} as

$$N\left(cm^{-2}\right)=\frac{\Delta V_{fb}\varepsilon_{ox}}{qd_{0x}} \tag{1}$$

where q is the electronic charge, ε_{ox} is the oxide dielectric constant, and d_{ox} is the oxide thickness.

A model by Tsetseris et al. [4] suggests that interface trap buildup during NBTI can be fit to the sum of an exponential and a power law in time, with an exponent of 0.25. The data we show here are for the total flatband shift, which contains trapped charge as well as part of the interface state distribution, but we have nevertheless fit our data to this model, with the result in shown in Figure 5b. The parameters for this fit are also found in Table 2.

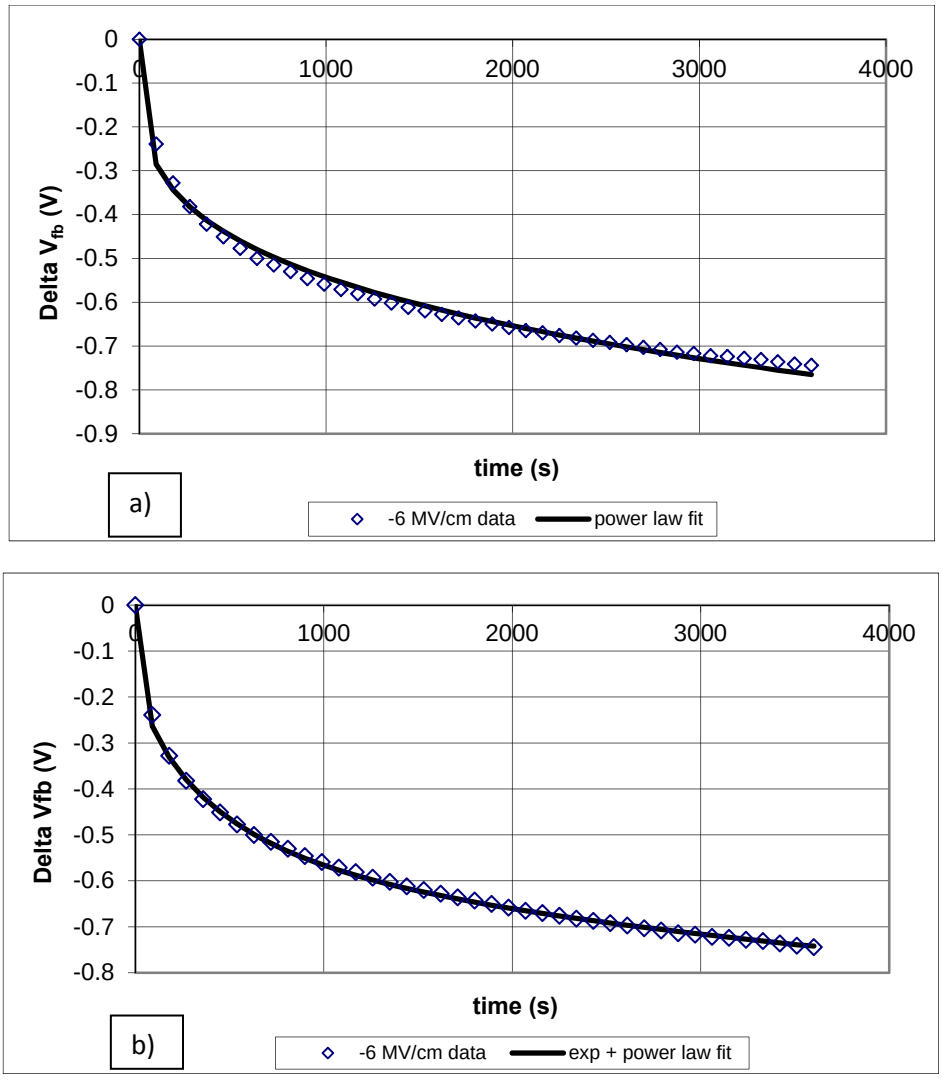


Figure 5. Fit to -6 MV/cm data of Figure 1. a) Power law in time: at^n with a = -0.085 V and n = 0.268. b) Sum of exponential and power law: $a[1 - \exp(-bt)] + ct^{0.25}$ with a = -0.154 V, b = 2.32 x 10^{-3}, and c = -0.76 V.

Table 2. NBTI parameters for the models discussed in the text.

Field (MV/cm)	Power Law $\Delta V_{fb}(t) = a.t^n$		Exponential + Power Law $\Delta V_{fb}(t) = a.[1 - \exp(-bt)] + c.t^{0.25}$		
	a (V)	n	a (V)	b (s^{-1})	c (V)
-4	-0.088	0.210	-0.111	2.27×10^{-3}	-0.050
-5	-0.092	0.252	-0.171	1.86×10^{-3}	-0.067
-6	-0.085	0.268	-0.154	2.32×10^{-3}	-0.076
-7	-0.211	0.254	-0.393	2.55×10^{-3}	-0.162

The Tsetseris model predicts that interface trap buildup is exponential (reaction limited) at small stress times and diffusion limited at later times ($t^{0.25}$). Using the results in Table 2, we assume first order kinetics $N \propto 1 - e^{-k_f t}$ and take an average value for b of 0.00225 s, which gives $k_f = 444\ s^{-1}$. By comparison, the "back of the envelope" value provided in Eqn. 4 of reference [4] gives $k_f = 64$ (for a H depassivation barrier height of 1 eV, an attempt frequency of 10^{13}, and T = 150°C), so our result is a little off, possibly reflecting the fact that we have not subtracted out the trapped charge in these data, or else that the approximations in reference [4] are not appropriate here.

We do not comment on kinetics beyond this simple characterization, because we feel that extracting kinetics using CV data (flatband voltage shifts on MOS capacitors) is not accurate. As we will show later, and as is well known in the literature, the positive charge induced NBTI stress is lost very rapidly once stress is removed. On the time scale necessary for our apparatus to record a flatband voltage shift (~1 s), a very large portion (~25%) of the induced charge may have been lost. Therefore we do not use V_{fb} kinetics data except to show that our results are similar to what is found in the literature, and to show that the charge/discharge cycle is not like that for APC (Section 4.1.2). More accurate kinetics can be derived from "on-the-fly" measurements, such as those discussed in Section 4.4 below.

We have also looked at interface trap density following NBTI. Figure 6 shows the interface trap distribution (D_{it} $cm^{-2}eV^{-1}$) obtained from comparison of the high frequency and quasi-static CV curves. The sample had been stressed at -5 MV/cm and 150°C for a total of 3600sec, but the CV measurements used to generate the interface state data were done at room temperature, after NBTI stress had concluded. The D_{it} distribution shown here is similar to that reported in the literature, i.e., there is a slight peak at roughly mid-gap. It is also similar to D_{it} spectra obtained under other stress conditions.

The CV comparison method used to generate D_{it} spectra provide data only from approximately 0.4 eV to 0.8 eV, as can be seen in Figure 6. Outside that range, the technique is

not accurate. Therefore it is difficult to assess the total interface state density (by integrating over the band gap) unless assumptions are made as to the spectrum outside the usable range.

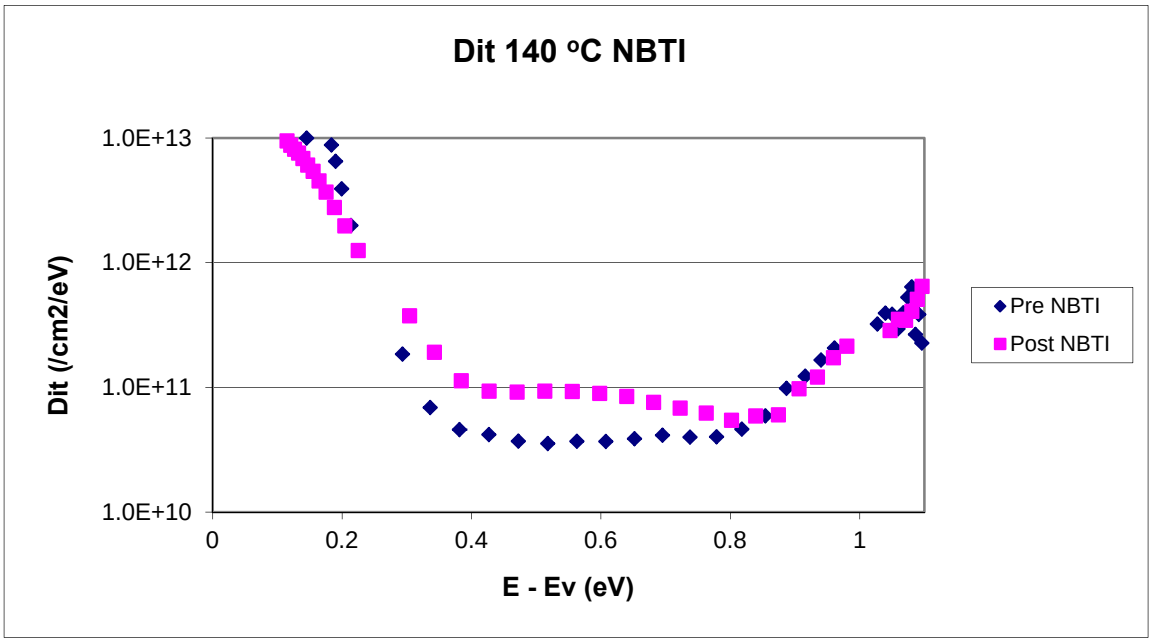


Figure 6. Interface trap density from a high-frequency/quasi-static CV comparison.

4.1.2 Comparison of NBTI Charge/Discharge Kinetics with APC and Trapped Holes

An important result from this work concerning the nature of positive charge induced by the NBTI in Al-gate MOS capacitors is that this defect is a trapped hole, for which the trap depth is approximately 0.3 eV. It is not, as was posed initially as a working hypothesis in our proposal, due to anomalous positive charge (APC).

The first step in establishing this conclusion was demonstrating that the qualitative behavior of NBTI-induced defects is not at all similar to that for APC. The conclusion was further supported by data showing that the discharge kinetics following NBTI stress are more like the loss of trapped holes than like the charge/discharge of APC. Specifically, discharge kinetics show that on removal of stress, positive charge is lost very quickly, even at elevated temperature. This is expected if charge is due to trapped holes, which will leave the sample rapidly when stress is removed.

As discussed in Section 3.4, APC defects are characterized by a reversible charge/discharge cycle: electrons can be induced to flow into and out of them by application of an appropriate gate bias. The charging and discharging of APC is observed as a change in the flatband voltage V_{fb} in response to gate bias: positive bias brings electrons to the surface, neutralizing the positive charge and causing an increase in V_{fb}, whereas negative bias empties the defects and decreases the flatband voltage.

Figure 7 shows application of an alternating bias of +/- 2 MV/cm to a sample having previously undergone the NBTI stress at -6 MV/cm and 150 ^{o}C. (The field used here to probe for APC is smaller than that shown in Figure 2, but we have other data at +/- 4.5 MV/cm that are

virtually identical to Figure 7.) We do in fact observe an alternating shift in the flatband voltage; however, similar shifts are observed in as-grown (undamaged) samples. More to the point, the shift is in a direction *opposite* to that for APC: compare the direction of the shifts during application of positive bias for Figures 2 and 7. Further, after application of the first positive bias, there is relatively little shift in the flatband voltage, even relative to the as-grown samples. This and similar measurements lead us to conclude that under the NBTI conditions used here, APC is not being generated.

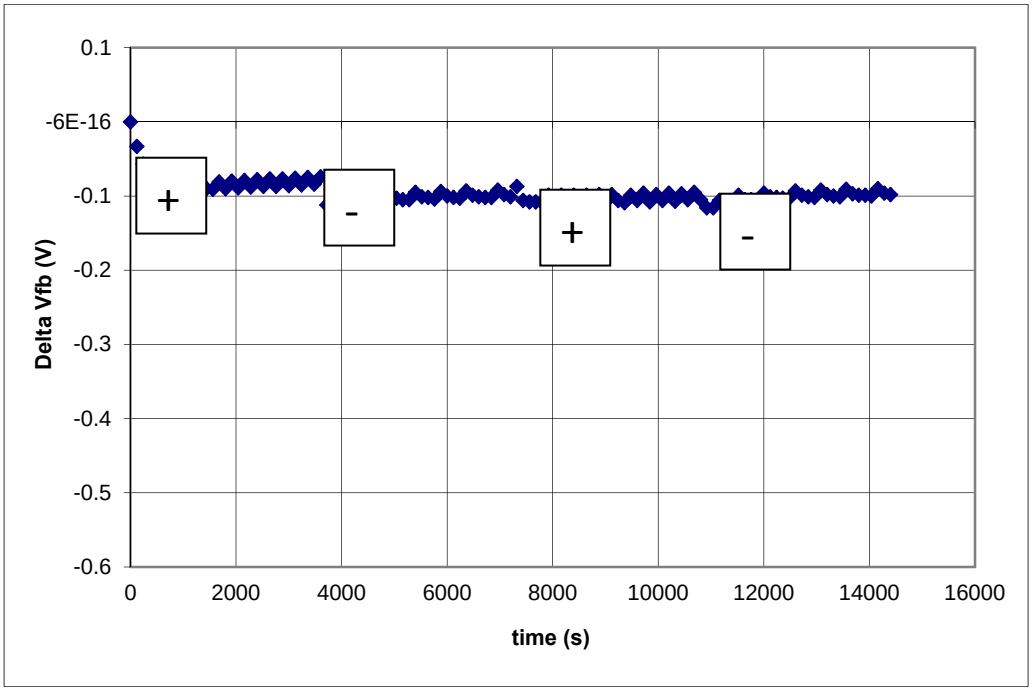


Figure 7. Probe for APC on a sample stressed at -6 MV/cm and 150 ^{o}C for 7200 sec.

Figure 8 shows additional data taken to determine the time dependence of the relaxation of positive charge, and thus to compare it to APC and trapped holes. In both experiments shown, the flatband voltage (here converted to charge density using Equation 1) is being tracked as a function of time during NBTI stress at -4 MV/cm and 150^{o}C. The upper graph provides a good example of the extent and rapidity of charge relaxation when the applied voltage is reduced to 0 (but note that the temperature remains at 150^{o}C). In the lower figure, we show what happens when the stress is re-applied, and then released once again: the original defects are almost recovered (with approximately the same kinetics) when the stress is re-applied, and the relaxation is again observed when the stress is removed. While we cannot be quantitative because the CV flatband measurements are too course, it is clear that charge is lost and recovered very rapidly. This is characteristic of trapped holes, but decidedly not characteristic of APC.

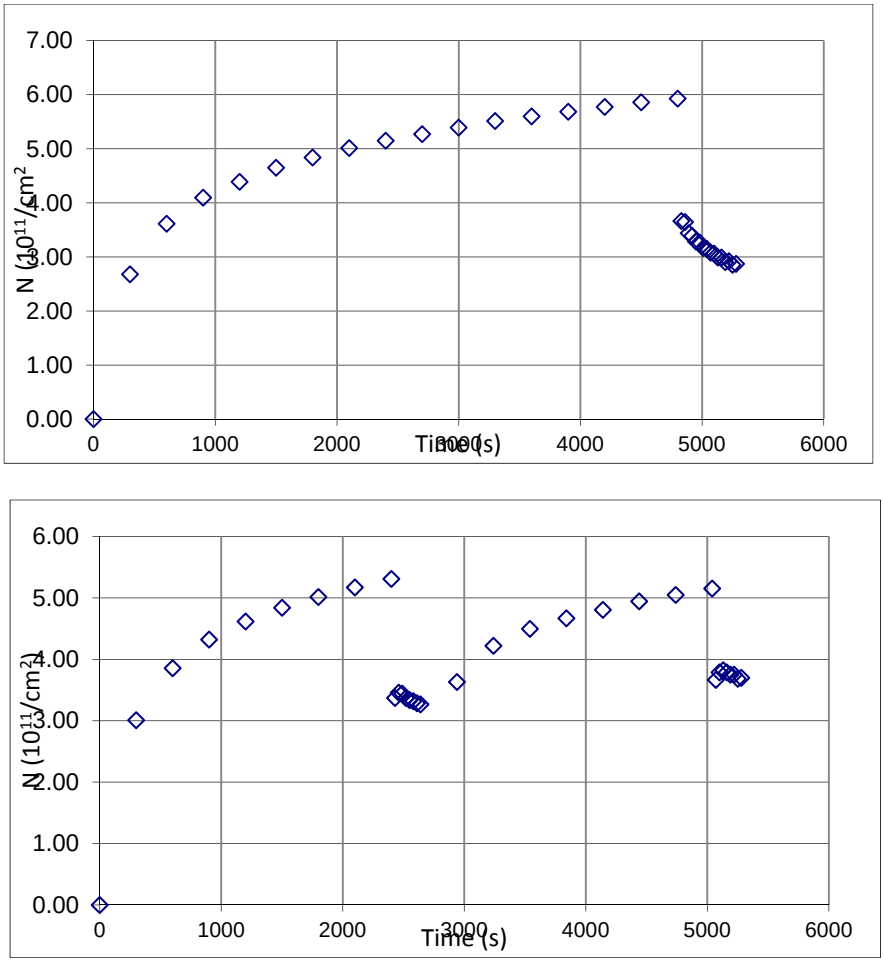


Figure 8. Discharge of NBTI-induced charge on removal of bias.

4.1.3 Temperature/Bias Dependence of Charge Population

One of the more interesting observations concerning the nature of NBTI-induced charge was that following NBTI stress, if the sample is cooled but the bias is maintained at the stress value, most of the charge is lost anyway. In other words, bias alone is not sufficient to maintain charge in the oxide; an elevated temperature is also required.

Figure 9 shows NBTI charging curves (flatband voltage V_{fb} vs. time) on MOS capacitors with 39 nm SiO_2 insulators. The gate stress was -4.5 MV/cm; the stress temperature for a given curve varies from 100°C to 175°C. Flatband voltage V_{fb} measurements were taken during stressing every 60 s for approximately 3600 s; at that time the measurement interval was reduced to 20 s (to improve time resolution for the cooling period) until a total elapsed time of 4100 s, at which point the temperature was reduced by water-cooling of the chuck. The chuck temperature minimized several degrees below room temperature after approximately 140 s, and then stabilized to room temperature after another 200 s; this overshoot accounts for the slight reduction of V_{fb} after reaching a peak, as is observed in the higher temperature curves. During cooling, the gate voltage (-4.5 MV/cm) was maintained at all times.

From Figure 9 we observe that the flatband voltage decreases due to the bias-temperature stress, but increases (becomes more positive) during cooling, even though gate voltage is maintained. Approximately half of the change in V_{fb} is due to temperature dependence in the flatband voltage itself; we interpret the remainder as being due to a loss of positive charge.

Figure 10 shows the change in V_{fb} with temperature when a gate voltage of 0 V (i.e., no voltage stress) is applied; this data measures the change in V_{fb} due to temperature alone. An overshoot during the cooling cycles is again noted.

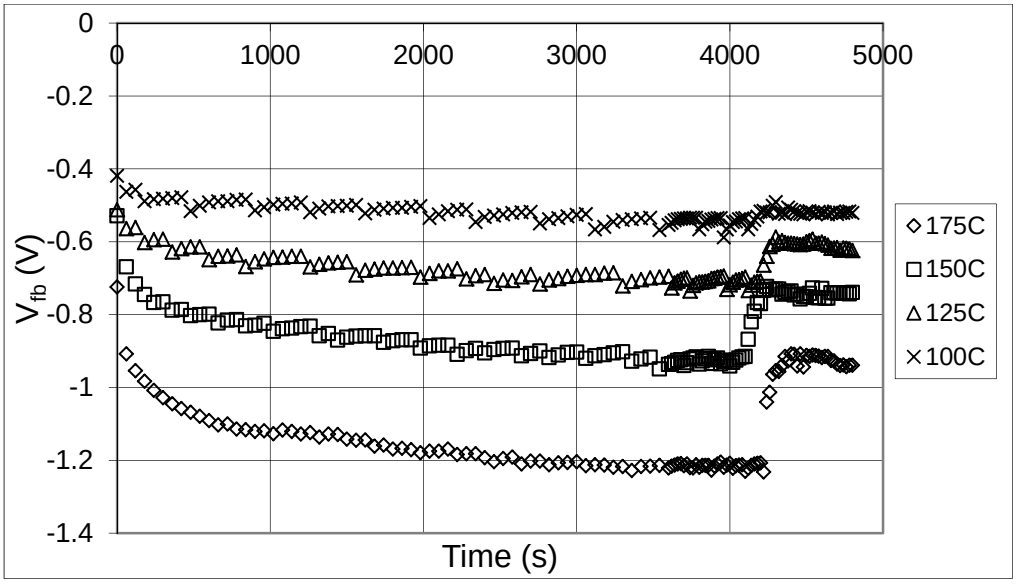


Figure 9. Flatband voltage shift vs. time during NBTI stressing at -4.5 MV/cm and varying temperature.

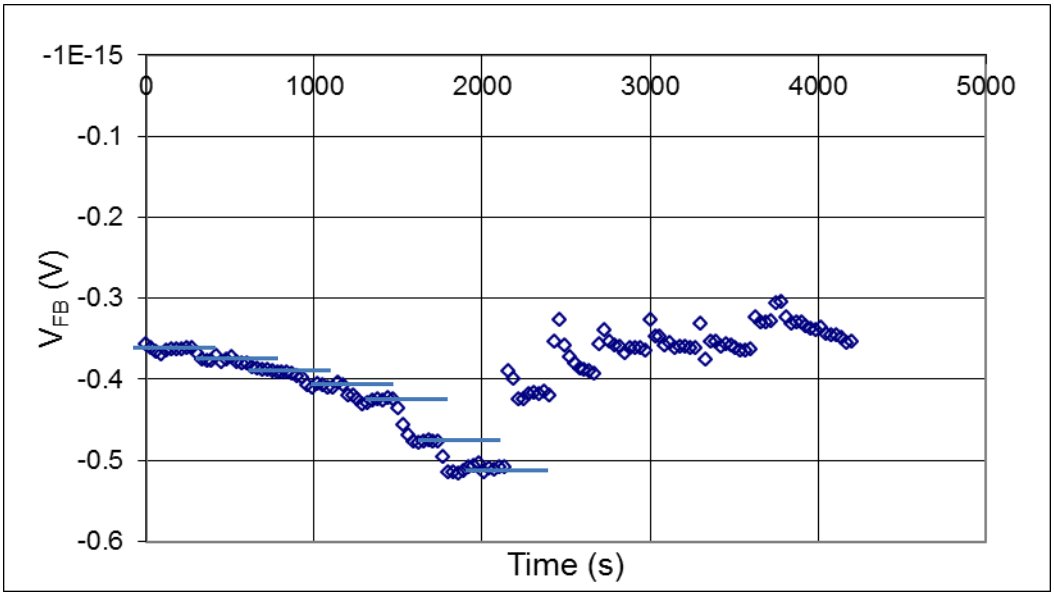


Figure 10. NBTI "stress" curve with 0 gate voltage applied, reflecting the temperature dependence of V_{fb}.

To obtain the data in Figure 9, V_{fb} measurements were made for approximately 400 s, at which point the temperature was changed. Until 2200 s, the temperature is increasing in the steps 23, 50, 75, 100, 125, 150, and 175°C. The horizontal lines indicate the stabilization points at each temperature. For the remainder of the experiment, the chuck is cooled sequentially to the same values. During cooling there is considerable overshoot in the temperature control, which accounts for the spikes in the data.

In Table 3 we list the total change in V_{fb} (ΔV_{fb} total) determined from Figure 9, the change in V_{fb} due to temperature alone ΔV_{fb} (T) determined from Figure 10, and the result of the subtraction, that is,

$$\Delta V_{fb} \text{ total} - \Delta V_{fb} (T) = \Delta V_{fb} (+). \quad (2)$$

We interpret ΔV_{fb} (+) as the change in V_{fb} due to loss of positive charge. For the 100°C curve, we find that the change in V_{fb} is due almost entirely to temperature alone. For the higher temperatures, there is a change due to loss of charge.

Table 3. Shifts in the flatband voltage on cooling.

	175 C	150 C	125 C	100 C
ΔV_{fb} total [V]	0.282	0.189	0.113	0.038
ΔV_{fb} (T) [V]	0.152	0.119	0.062	0.045
ΔV_{fb} (+) [V]	0.13	0.07	0.051	-0.007

To account for these observations, we suggest that a shallow hole trapping site very near the Si-SiO_2 interface exists, and fills quickly when holes are present and thermal energy (above room temperature energy) is applied; in other words, trapping is a thermally assisted process. A bias is required to bring holes to the interface, and temperature is required because the trapping process is thermally assisted. On the scale of our flatband voltage measurements this process may be, for all practical purposes, instantaneous. The occupancy of the traps is thus in dynamic equilibrium, with hole trapping and de-trapping taking place simultaneously and continuously. Removal of either bias or temperature means that only de-trapping can take place, but the trapping is quickly restored when the bias/temperature is restored.

In this scenario, the change in the flatband voltage ΔV_{fb} (+) is a measure of the charge that was trapped via the proposed thermally assisted process. We further assume that this process follows an Arrhenius-type behavior. Accordingly, the data are plotted in Figure 11, which indicates an activation energy of 0.29 eV.

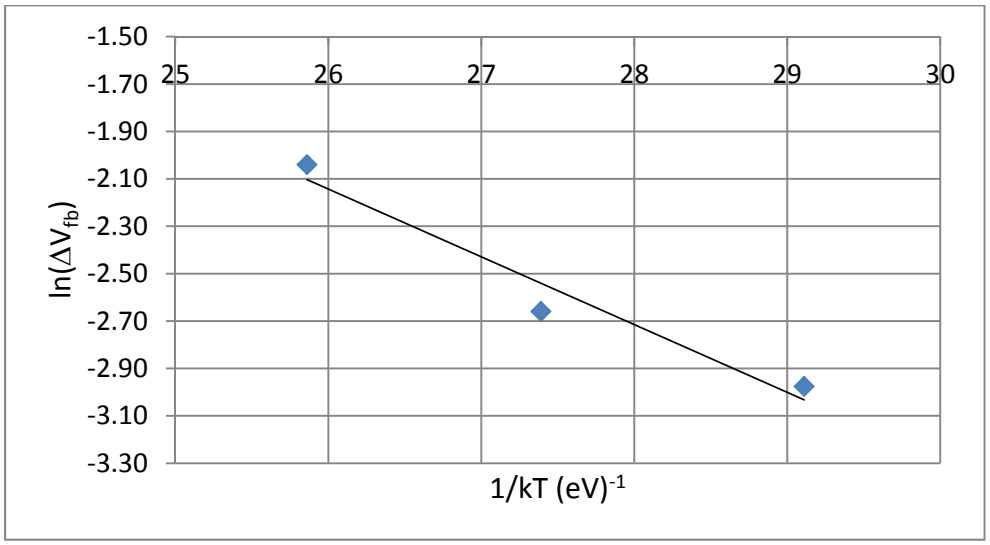


Figure 11. Arrhenius plot of the change in flatband voltage.

4.2 Computer Modeling of the Si-SiO_2 Interface

We completed simulation of the electric field strength at the Si-SiO_2 interface using Silvaco's Virtual Wafer Fab software. We simulated a 3 nm oxide under negative bias stress (at room temperature). The purpose of the investigation was to determine whether the model for NBTI damage proposed by Tsetseris et al. was plausible. We found that it was indeed plausible based on the value and sign of the electric field at the interface, but that it is not possible to say whether the model is correct, i.e., that what is plausible is indeed occurring.

An important feature of the model proposed by Tsetseris, et al., is that the electric field in the substrate pulls H^+ to the interface, where it is trapped to form positive oxide charge. In addition, it may diffuse along the interface to and de-passivate dangling Si bonds, thus producing interface states. The origin of the H^+ species is the result of a two-step process: (i) removal of H

from a donor-hydrogen complex upon capture of a hole ($H^- \rightarrow H$), followed by (ii) hole capture to generate H^+. The holes are supplied by the inversion layer at the interface.

The Tsetseris model has two important premises: that H+ can be generated in the depletion/inversion region and remain stable long enough to do damage, and that the electric field varies sufficiently, even in inversion, to account for the gate bias dependence observed in NBTI experiments. To evaluate the viability of the model, we describe computer simulations performed using Silvaco's *Virtual Wafer Fab* (VWF) software to model the electric field at the interface.

Our simulations involve a simple MOS capacitor with constant phosphorous substrate doping of 2 x 10^{16} cm^{-3}, and an SiO_2 thickness of 2.3 nm. Our model includes Fermi-Dirac statistics in the evaluation of the electrical properties, but it does not include quantum effects, notably gate oxide tunneling, although we do not expect that to affect the results given here.

In Figure 12 we show a typical simulation of the potential and the electric field across the device for an applied bias of -1 V. Figure 12a shows the surface electric field (E_s) in the substrate and the gate voltage (V_g) as a function of the surface potential (Phis). Figure 12b shows the surface electric field (Es) as a function of gate voltage (V_g). We see that the surface potential becomes fixed at a gate voltage of approximately -1.2 V (corresponding to inversion), but that the field at the interface does indeed vary with gate bias beyond inversion. We also note the depth to which the field penetrates the substrate (approximately 400 nm). We can make only the qualitative statements that (i) the electric field is in a direction to draw H^+ to the interface, and changes substantially with gate voltage beyond inversion, and (ii) there appears to be a sufficient volume in which to generate H^+, assuming such a species is stable.

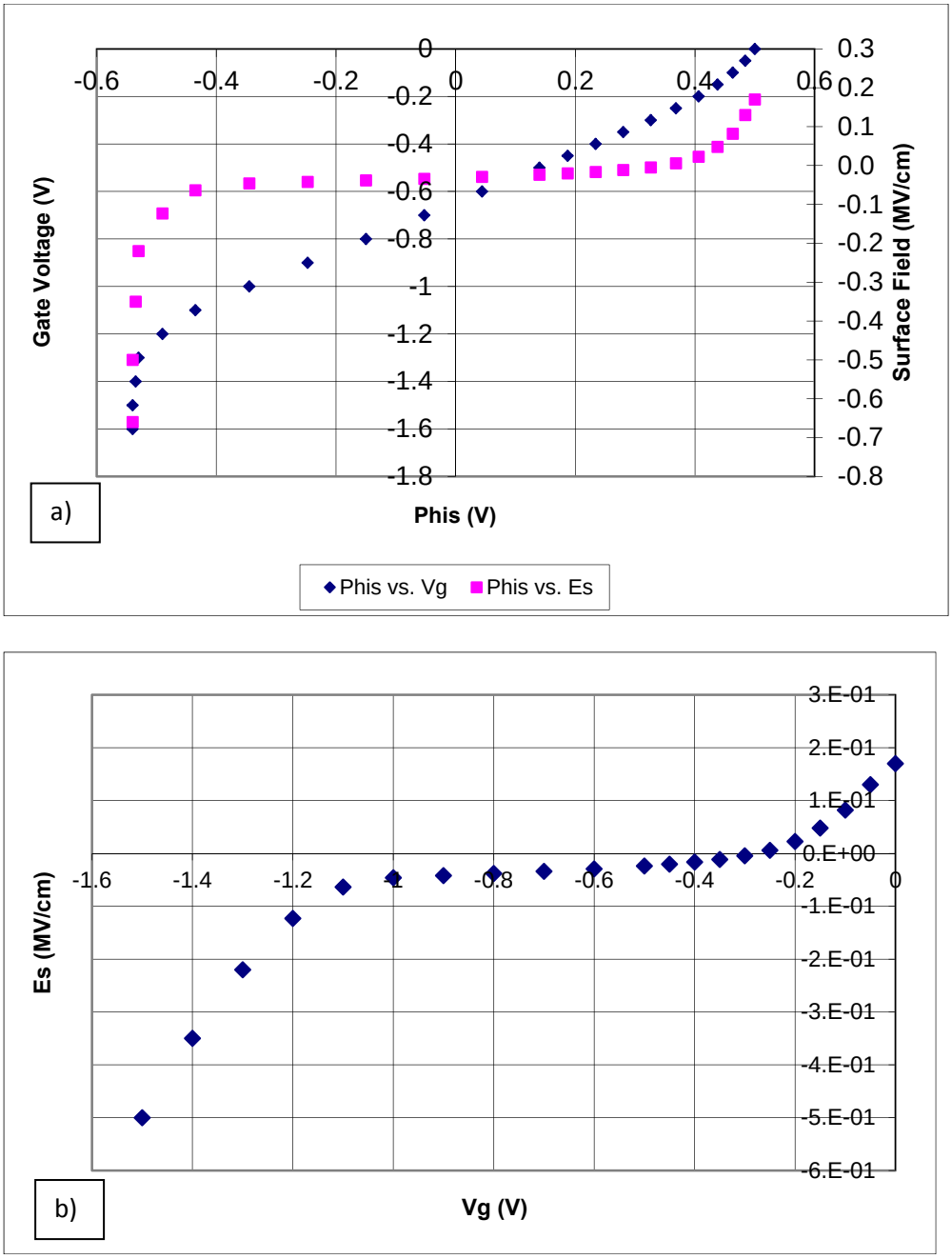


Figure 12. a) Gate voltage and surface field (electric field at the Si-SiO_2 interface in the substrate) as a function of surface potential. b) Surface field as a function of gate voltage.

4.3 Attempt at Reduction of Charging via He Implantation

We hypothesized that injection of He ions into the oxide following oxidation would reduce the density of NBTI-induced defects. The idea was that the presence of He in the oxide might disrupt either the transport of holes or the transport of hydrogen. Hydrogen might be expected to play a role in degradation if the dominant mechanism for defect generation is a de-

passivation process that creates interface states. To that end, we implanted samples with He at several doses using an implanter available in-house. The results showed that there was no significant difference in the NBTI charging kinetics of samples with or without He. We conclude that this method of reducing NBTI damage is not likely to be successful.

To conduct this test, we first established from TRIM calculations the conditions necessary for implantation of He ions into the MOS oxide. We then fabricated an oxide and implanted He at 5.2 keV, and characterized the He implanted sample with regard to NBTI defect generation kinetics. We compared the results with those from a sample that was not subjected to He implantation. We did not attempt to optimize the implant conditions. Nevertheless, we emerge with a rational protocol for future implantations, and some preliminary results.

The sample to be implanted was fabricated in our lab by oxidizing n-type Si to a thickness of 35.6 nm, and covering with 70 nm of PMMA via spin-coating. It was then exposed to a He ion beam at an energy of 5.2 keV (nominally) and a current density of 150 nA/cm^2 for a time varying between 5 and 60 sec.

Following implantation, the PMMA was etched off, and circular Al dots (2.67 x 10^{-3} cm^2 area) were thermally evaporated onto the implanted oxide for electrical measurements. We were not able to "map" the position of the beam very accurately to the position of the metal dots, and so the implant dose received by the dots on which we performed NBTI experiments is not well known. However, based on the current density and exposure time, the implant dose was in the neighborhood of 2 x 10^{13} cm^{-2}.

TRIM calculations, shown in Figure 13, indicated that a beam energy of 5.2 keV would put the center of the He ion distribution in the center of the oxide.

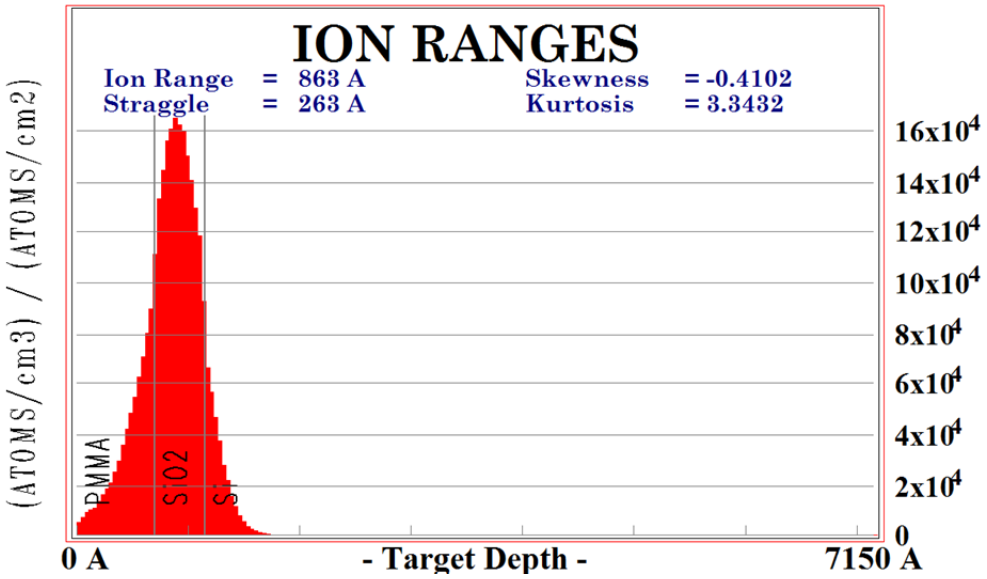


Figure 13. TRIM calculations showing location of He ions implanted at 5.2 keV through 70 nm of PMMA on 35.6 nm SiO_2.

We have done TRIM calculations for energies varying from 5.85 keV to 3.9 keV. This range of energies puts the peak of the He distribution in the oxide, although its position varies across the oxide thickness; in other words, 5.85 keV puts the He distribution peak near the Si-

SiO_2 interface, and 3.9 keV puts it near the metal-SiO_2 interface. This is an important result, because in doing the implants, the single biggest experimental uncertainty concerning the ion distribution is the beam energy. There is also a large (probably 25%) uncertainty in the dose, which arises primarily because the number of neutral atoms in the beam can only be estimated; but beam current measures ions only.

Figure 14 shows four NBTI curves taken on separate capacitors on a sample called "40909" at -4 MV/cm and 150 ^{o}C. Superimposed on this data are two additional runs on the He-implanted sample. The spread in the kinetics for 40909 represents our capacitor-to-capacitor variation for this sample. The He-implanted results (taken on a different sample) span the non-implanted results, showing that there has been no change in NBTI response due to He implantation.

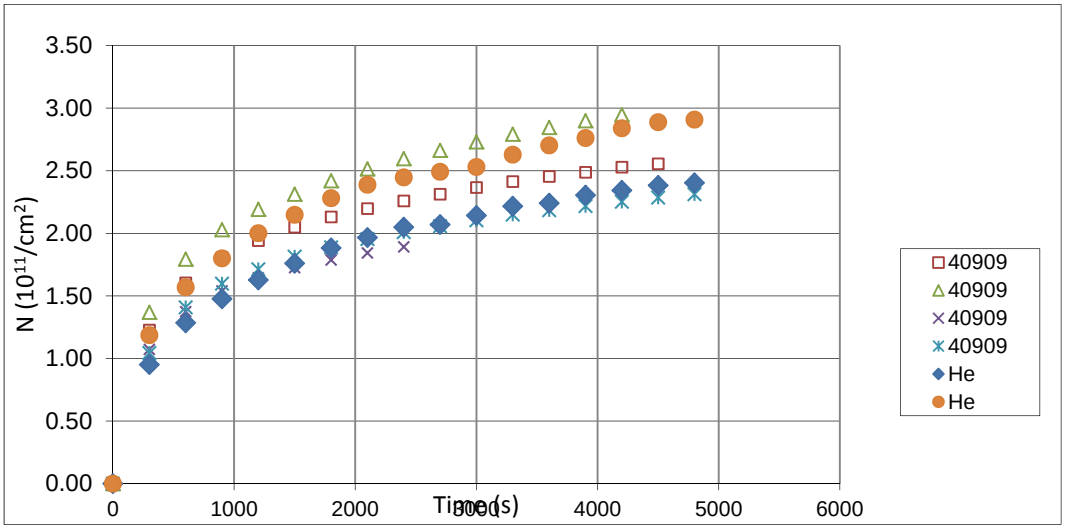


Figure 14. Charging kinetics for NBTI at -4 MV/cm and 150^{o}C.

4.4 NBTI in HfSiON MOSFETS

During the spring of 2010, the PI (Dr. Trombetta) was on sabbatical at AFRL. He worked closely with Dr. Roderick Devine on measurement of HfSiON MOSFETs. These measurements are "on-the-fly", in that measurement of damage can be done without removing the NBTI stress. This is possible in MOSFETs because the drain current can be measured while stress, which is applied at the gate, remains unchanged. [5]

Using a Keithley 2400 system at Kirtland, Dr. Rod Devine, Mr. Jessie Mee, and Dr. Len Trombetta made NBTI measurements of 1 μm gate length MOSFETS with HfSiON gate insulators. In these experiments, MOSFETS were stressed at a particular gate bias and at elevated temperature, and the drain current was monitored as a function of time. From the drain current data, the MOSFET threshold voltage V_{th} was extracted using a simple model for the current-voltage characteristics of the MOSFET (i.e., the Square Law Model). Since this measurement is done during device operation, there is no interruption required to make a measurement of oxide charging, as there is in the case of the MOS capacitor. Thus the

measurement technique ensures that no charge is lost due to the measurement technique (i.e., they are "on-the-fly"). However, there is one caveat: the first data point requires approximately 2 s to be made, so it is necessary to extrapolate the charging curve (V_{th} vs. time) to t = 0 in order to obtain charging kinetics. After that, measurements can be made at time intervals as short as tenths of seconds. In general, measurements using the Keithley system were made approximately 0.7 s apart.

In using the Keithley system to measure NBTI charging kinetics on HfSiON MOSFETs, we discovered that the kinetics depend on the drain voltage used to operate the device. Figure 15 shows this effect: the drain voltage V_{ds} is varied from -0.1 V, where the device is operating in the linear region, to -2.0 V, where the device is in saturation.

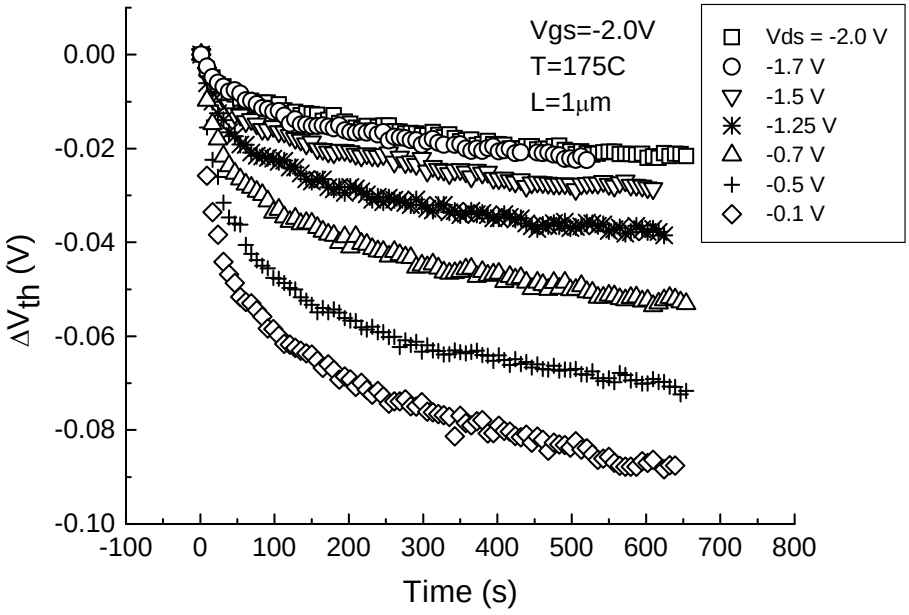


Figure 15. Threshold voltage shift in HfSiON based devices measured for NBTI stress at a gate-source voltage V_{gs} = -2.0 V, T = 175°C, and varying V_{ds} as indicated.

There is nothing in the literature that we could find to explain this observation, and indeed data of this type has not been reported, to our knowledge. Further, preliminary measurements by Devine and Trombetta on MOSFETs with SiO_2 insulators suggested that the effect does not take place in these devices; in other words, the dependence of the charging curve on drain voltage appears only in the high-k dielectric devices. Subsequently, Devine and Mee made more complete measurements on SiO_2 devices and confirmed the preliminary results.

The work done while at AFRL were published in the journal *Microelectronic Reliability*. [6] The publication reported that positive charge induced by NBTI in HfSiO MOSFETs is less severe when the MOSFET is operated in the saturation region (high drain bias) than when it is operated in the liner region (low drain bias).

To explain the effect of drain voltage, we postulated that (i) positive charge was being trapped either in the high-k insulator or at its interface with the SiO_2 layer beneath it; (ii) the positive charge trapped in these regions is highly mobile in a lateral direction, i.e., along the

channel. The model then states that during measurement, the positive charge is moving in the direction of the drain (through the insulator or along the interface) and exiting the drain. This de-trapping mechanism does not exist in SiO_2 devices because the charge is only mobile when the high-k material is present.

The devices used to take the data of Figure 15 had a very high substrate doping density (~ 10^{18} cm^{-3}) and a very thin dielectric (equivalent oxide thickness approximately 2 nm), and therefore were not expected to exhibit short channel effects. Numerical modeling confirmed this conclusion, as did measurements intended to reveal short channel effects (which were not detected). Therefore we were able to rule out short channel effects as an explanation for the observations.

4.5 Attempt at Reduction of Charging via Oxygen Anneal

In an effort to determine whether NBTI charging is due (at least in part) to a lack of oxygen at the Si-SiO_2 interface, we designed a set of oxygen anneal experiments. In these experiments, an oxidized Si wafer is placed in a Rapid Thermal Processor (RTP) and annealed in oxygen. The anneal was done in pure O_2 at temperatures ranging from 900 to 1000^{o}C and for times ranging from 8 to 15 seconds. The intention is to "heal" oxygen-deficient sites (defects) at the Si-SiO_2 interface. [7] For this portion of the work, we used wafers that had been oxidized by University Wafer because our oxidation furnaces were producing unreliable samples (see Section 3.1).

Unfortunately, our measurements are inconclusive. In some cases it was clear that the oxygen anneal was too aggressive, and probably created additional SiO_2, thus defeating the purpose of the anneal. For example, following a 1000 ^{o}C 15 s anneal in O_2, the sample thickness of 30 nm increased to approximately 35 nm. But regardless of whether the thickness increased or not, we observed anomalous NBTI results, suggesting that the RTP unit is contaminated, and that it introduced defects into the oxide.

Results typical of NBTI runs on RTP samples are shown in Figure 16. This figure shows raw data, i.e., no subtraction of the initial flatband voltage has been made. All three NBTI runs were taken at a stress of -5 MV/cm and at a temperature of 170^{o}C. The diamond markers show a control sample, i.e., one with no anneal. The other curves show data for two different anneals. The NBTI curve for the control sample is typical of what we have been observing. Temperature is elevated beginning at approximately 800 s, so the data before that time are taken at room temperature. When the temperature is elevated, beginning the NBTI run, the flatband voltage shifts to more negative values, as is typical of NBTI data. However, data for the sample annealed at 1000^{o}C in O_2 (squares) is completely anomalous: the flatband shifts upward dramatically, instead of downward, as would be the case for NBTI damage. To test whether the oxygen anneal is causing this behavior, we run a third sample annealed in N_2 for 8 s. It too is anomalous, although not as dramatically so as the longer oxygen anneal sample, probably because of the lower time.

The most likely explanation for the data shown in Figure 16 is that the RTP is introducing contaminants into the oxide; these contaminants have an electrical signature of their own that is overwhelming the NBTI response of the sample. We attempted to "fix" this by doing a PMA following the oxygen anneal, but this was not successful. We have also lowered the NBTI stress

temperature to 900°C. Although the lower temperature reduces the extent of the anomaly, we still do not observe normal NBTI behavior.

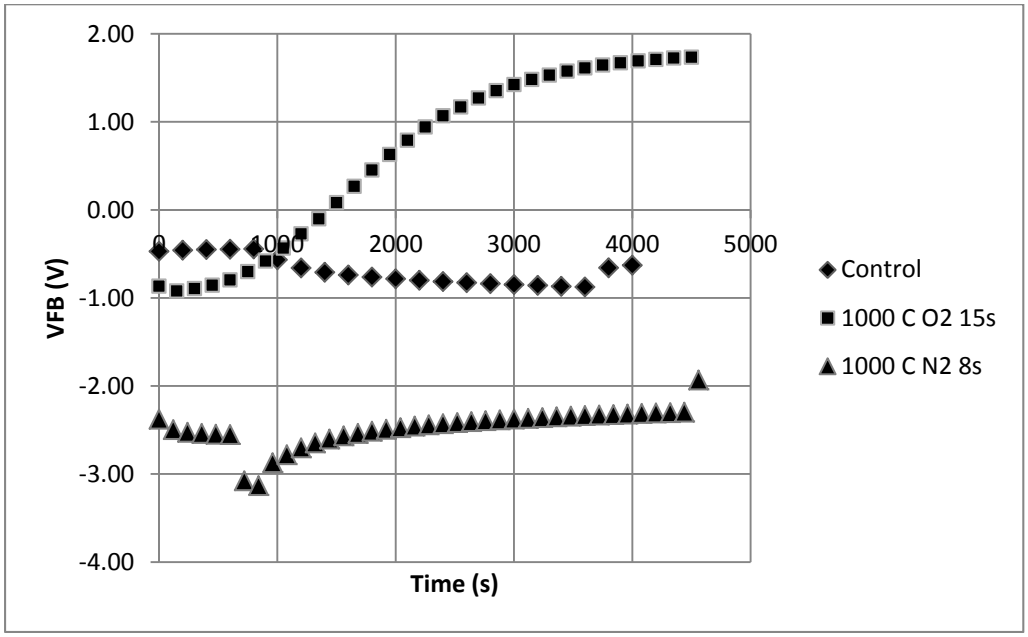


Figure 16. NBTI data for a control sample, as well as a sample annealed at 1000°C for 15 s in O_2, and another annealed in N_2 for 8 s.

4.6 Student Support

The project supported two students who successfully earned a MSEE degree as a result. The first graduated in December 2009. This student is currently pursuing a PhD at Vanderbilt University. The second student graduated in May 2011 and is currently working in the semiconductor industry.

4.7 Work Not Completed

There were several tasks associated with the work that were not completed, largely because of time limitations or an inability to procure samples. We unfortunately had to spend a great deal of time repairing equipment, including the RTP. In addition, the laboratory in which we fabricate our samples was inoperative while repairs to the infrastructure were being made, and these repairs took considerably longer than anticipated.

4.7.1 Radiation Experiments

Radiation experiments were to be carried out on samples treated using He implantation and oxygen annealing. We were not able to complete these experiments. On the other hand, it would appear that there would not have been a great deal of information to gained, since the He implantation did not produce the desired effect and the oxygen anneal experiments are so far inconclusive.

4.7.2 Computer Simulations

Computer simulations of the electric field at the Si-SiO2 interface were completed, as described above. However, we were also tasked with developing a simulation of a MOSFET structure designed for controlled injection of holes into the insulating region. The goal was to later build such a device for use in reliability studies at AFRL. Because of time constraints brought on by the need for infrastructure and equipment repair, we were not able to complete these studies.

5.0 CONCLUSIONS

This work sought fabrication methods to reduce the susceptibility of MOS devices to NBTI. We tried two methods to achieve this: implantation of He ions into the oxide layer, and oxygen annealing. In addition to investigating fabrication treatments to reduce NBTI, we developed a model for NBTS-induced charging based on several observations made in the course of the work. This model is discussed in Section 4.1.3.

Concerning fabrication methods, we conclude that implantation of He ions is not likely to reduce the susceptibility of MOS devices to NBTI damage. This suggests that a hydrogen-related mechanism, such as that occurring when the device is exposed to ionizing radiation or high field stress, is not in fact responsible for NBTI. Alternatively, the hydrogen may be coming from the substrate, as suggested by Tsetseris et al. Indeed, our computer simulations showed that the Tsetseris model is plausible, although we cannot conclude that it is correct in detail.

Our experiments on oxygen annealing were inconclusive, and we suspect that RTP contamination created defects that masked NBTI effects. Therefore, we are not able to conclude whether an anneal would be successful in reducing NBTI susceptibility. However, we suggest that future work may show that with the proper conditions of temperature and time, an oxygen anneal may in fact be effective in reducing NBTI damage.

6.0 RECOMMENDATIONS

We remain optimistic that an oxygen anneal carried out under the right conditions (temperature, time) may yet be successful in mediating NBTI charging. Unfortunately time constraints and equipment issues have precluded further experimentation in this area. We suggest, however, that this work be continued in the future.

The He ion implantation was not successful in reducing NBTI defects. However, it is conceivable that either the proper process window (dose, energy) was not identified, or else that a different species of ion may be better suited to blocking the charging mechanism. In particular, nitrogen is known to improve the interface properties in some oxides, although the precise dose and spatial distribution is critical to success. Additional experimentation in this area may be warranted, but is not within the scope of this work.

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GLOSSARY

Capacitance-voltage (CV) – A measurement of capacitance across a capacitor (MOS capacitor here) as the voltage across the capacitor is varied.

Flatband Voltage (Vfb) – The voltage that induces zero net charge in the underlying semiconductor.

Fowler-Nordheim Tunneling – An emission of electrons induced by a large electric field. The theory describing this was proposed by Ralph H. Fowler and Lothar Wolfgang Nordheim. Strictly, Fowler-Nordheim equations apply only to field emission from bulk metals and (with suitable modification) to other bulk crystalline solids, but they are often used (as a rough approximation) to describe field emission from other materials.

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) – An MOS field-effect transistor used for amplifying or switching electronic signals.

Metal-Oxide-Semiconductor (MOS) – A structure obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon on top of that. Since the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor with one of the electrodes replaced by a semiconductor. When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor.

Negative-Bias-Temperature Instability (NBTI) – A key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance.

Negative-Bias-Temperature Stress (NBTS) – Voltage and temperature stresses applied to an MOS device in order to induce NBTI, which is defined below.

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